PATENT ABSTRACTS OF JAPAN

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(54) INFORMATION RECORDING AND REPRODUCING METHOD

(57) Abstract:

PROBLEM TO BE SOLVED: To obtain an information recording and reproducing method which deals with a recording error while a recording delay is being suppressed to a minimum by a method wherein, when the recording error is generated, user data after data, to be recorded, onward and logic address information are recorded in such a way that their recording position is slipped backward by one block.

SOLUTION: In a recording operation, a microprocessor 604 generates logic address information which corresponds to a logic address, and the logic address information is given to a recording circuit 606. The recording circuit 606 encodes the logic address information together with user data so as to be recorded in a designated block on a DVD-RAM medium 610. When a recording error is generated, the user data and the logic address information are recorded as they are in such a way that their recording position is slipped backward by one block without being encoded again. In a reproducing operation, when a block which is in(71) Applicant: HITACHI LTD

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dicated by a designated reproducing-start logic address is reproduced, an operation which deals with the recording error is performed when the logic address information which is recorded in a reproducing block is not matched with the designated reproducing-start logic address.

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